Cycle Slip Cancellation by Increasing the PFD Detection Range in PLL Circuits

Fabian Leonardo Cabrera[1,2], *Elkim Roa*[1] *and Wilhelmus Van Noije*[2]
[1]Integrated Systems Laboratory LSI - Polytechnic School of São Paulo University – São Paulo, Brazil
[2]Research group on Integrated Circuits Design CIDIC - Industrial University of Santander – Bucaramanga, Colombia
E-mail: fabian@lsi.usp.br, elkim@cidic.uis.edu.co and noije@lsi.usp.br

***Abstract*— The cycle slip problem in Phase-Locked-Loop circuits is discussed in this article and a solution is presented. This solution consists of a Lock-Detector based circuit, which increases the detection range of the Phase-Frequency Detector. In order to verify the proposed circuit, a PLL in 0.35μm CMOS was designed and simulated. The PFD and charge pump have an area of 0.005mm^2 and consumes 238μW. The proposed circuit decreases the lock time by almost half of what is required by a conventional PFD, without altering the stability of the loop.**

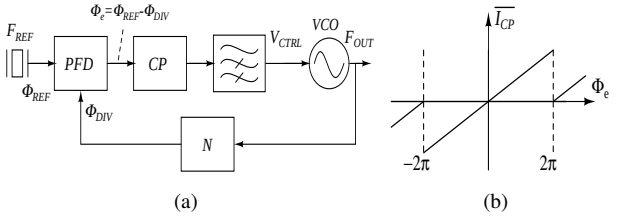

Fig. 1. (a) A conventional PLL diagram. (b) PFD transfer function.

I. INTRODUCTION

The Phase-Locked-Loop (PLL) is widely used in applications such as clock recovery, FM demodulation and frequency synthesizers. Regardless of the application, the time that it takes for the PLL to switch from one frequency to another, or lock time is an important specification in the design of the loop. Multi-standard receivers require PLL's to respond properly and quickly to wide frequency shifts with low phase noise and low spurs. To minimize phase noise, the loop bandwidth should be made as narrow as possible. However, the loop bandwidth should be made as wide as possible to get better tracking and acquisition properties.

In ideal conditions, lock time only depends on loop characteristics such as Voltage Controlled Oscillator (VCO) gain, charge pump current and the filter components. On the other hand, the limited detection range of the Phase-Frequency Detector (PFD) produces fluctuations on the control voltage of VCO, this undesired effect is called cycle slip, which can considerably increase the lock time. Figure 1a shows the diagram for a typical PLL. A change in the output frequency (F_{out}) can be produced by a change in either the reference frequency (F_{ref}) or the division module (N). If the phase error (Φ_e) is greater than 2π, the transient response of the PFD will restart at 0 due to the periodic nature of the phase, as shown in figure 1b. As a consequence, the control voltage will fluctuate increasing the lock time.

A possible first approach to avoid cycle slip is selecting a wide bandwidth, but it may be not feasible since it implies in greater phase noise in the output signal. Nevertheless, adaptive control schemes based on the phase error at the PFD, where the loop bandwidth increases with the phase error, have been reported [1]–[3]. A different solution is based on two tuning loops, where one loop works in wide phase differences and the other loop works as a free-tuning loop near the lock [4]. Instead of adaptive scheme, the latter solution added a second PFD as a discriminator-aided phase detector to increase charge pump current for a fast lock. In the cases mentioned before, the parameters of the loop are altered, affecting stability performance and consequently dependent specifications. A third novel solution presets the frequency of a mixed signal VCO depending on the divider ratio N [5]. In contrast to the others, this solution requires a pre-adjusted VCO, a presetting module, and compensation circuits which increase area and power. This paper describes a low area and low power alternative to reduce cycle slip without altering loop parameters.

The paper is organized as follows: The strategy to eliminate cycle slip is described in section 2. In section 3, a new PFD architecture which extends the linear detection range preserving the linearity of the loop at the frequencies of interest is presented. In addition, a prototype of PLL is designed and the simulation results are shown in section 4. Finally, the conclusions of the work are summarized in section 5.

II. STRATEGY TO ELIMINATE CYCLE SLIP

The strategy to prevent cycle slip concentrates on PFD and charge pump implementation. In this way, figure 2a shows the proposed PFD and charge pump organization. The PFD compares the reference signal (REF) with the signal that comes from the frequency divider (DIV), and generates two outputs (UP and DN) that control the current sources in the charge pump. Then, the charge pump injects or extracts charge from a filter, resulting in a voltage that controls the VCO. At the top of figure 2b the resulted step response of the loop can be seen. The second plot in figure 2b indicates the limited response

of the PFD without RED, while the bottom of figure 2b presents the response of the added blocks (the Range Extended Detector (RED) and the extra charge pump). Adding both currents results in the multiplication of the PFD linear range by two, as can be seen in figure 3.

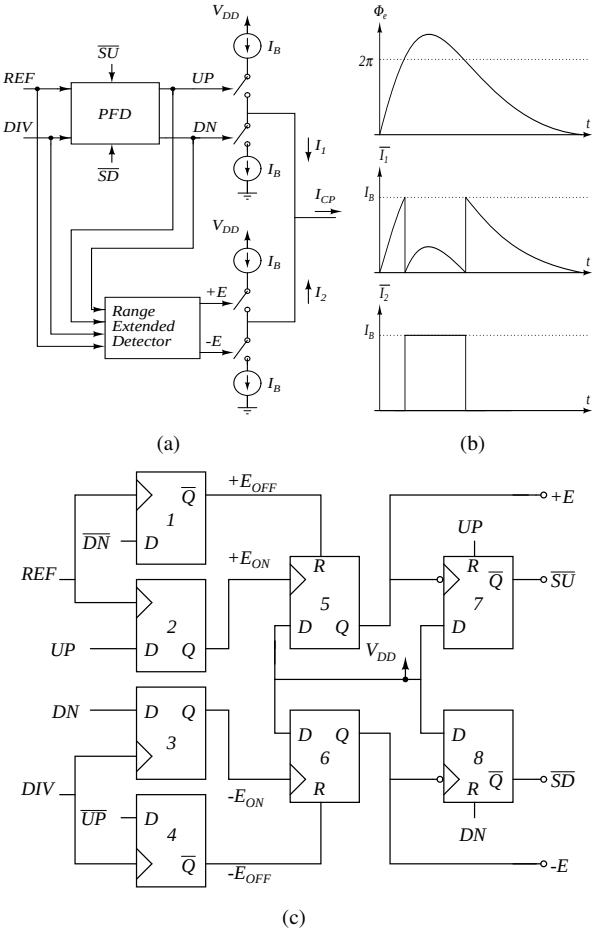

Fig. 2. (a) Proposed circuit. (b) Phase error and charge pump currents during a step transient response of the PLL. (c) RED Schematic.

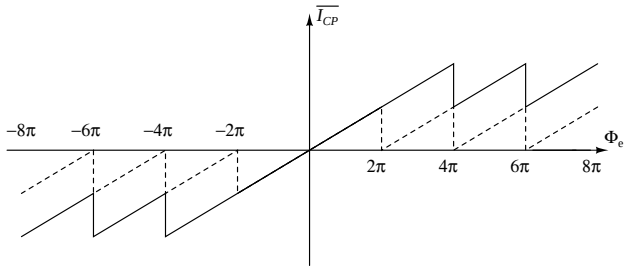

Fig. 3. PFD transfer function: with RED (solid line) and without RED (dashed line).

The function of the RED is to enable the second charge pump when the phase difference exceeds 2π, and later disable it when the phase difference becomes less than 2π. This can be done by using the circuit drawn in figure 2c. The core of the RED is the Lock Detector (LD) presented in [6]. Its function is to indicate when the phase error has reached the value of 2π where cycle slip starts.

The signals named SD and SU are necessary because they help the PFD to return the state where the phase difference was 2π, the point in which the second charge pump is disabled.

The use of RED as a strategy to cancel cycle slip enhances the PLL performance because:

- It is possible to multiply the detection range by two and the same idea may be extended to increase the range three or more times.
- The power consumption and the area occupied by the RED and the additional charge pump are relatively low.
- In steady state, the additional circuitry does not affect the performance of the PLL.
- The lock time is improved without altering the loop characteristics, such as gain or bandwidth.

The circuit is sensitive to the time between edges of input signals. Consequently, the RED occasionally activates the second charge pump for a few cycles before the phase error reaches 2π. However, this error is not significant in the transient response of PLL and can be suppressed for the operation frequencies.

III. Circuit Implementation

In order to verify the proposed circuit, a PLL has been designed in 0.35μm CMOS process. The implemented system is shown in figure 4.

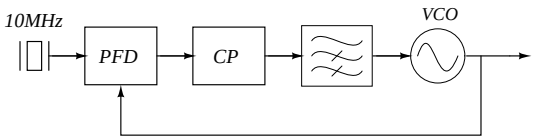

Fig. 4. Block diagram of implemented PLL.

1) PFD and RED: The schematic of the PFD can be viewed in figure 5a. The D flip-flop implemented in TSPC logic, shown in figure 5b, is a modification of that used in [7]. Flip-flops 1 to 6 in the RED block (figure 2c) were implemented in static logic, because its operation frequency is relatively low; the others employ dynamic logic like the flip-flop of the figure 5b.

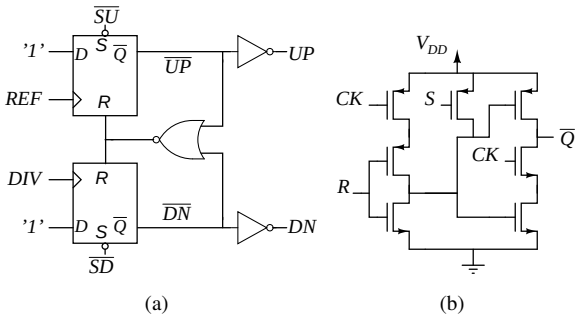

Fig. 5. (a) PFD Schematic. (b) $Flip\text{-}flop$ used in PFD.

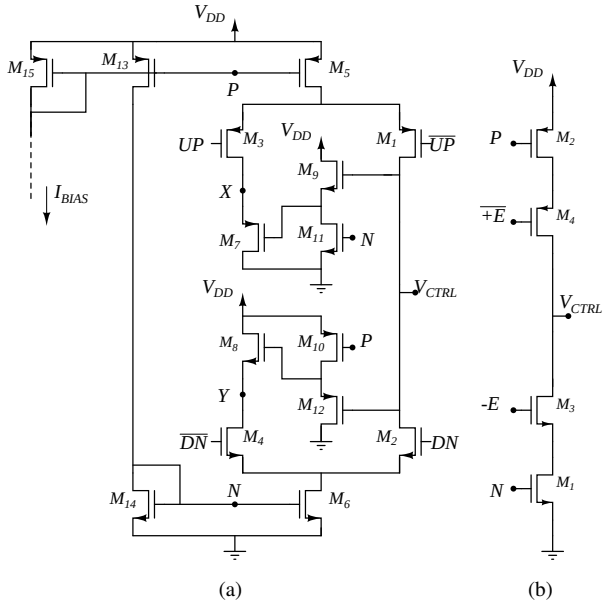

Fig. 6. Charge pump implemented.

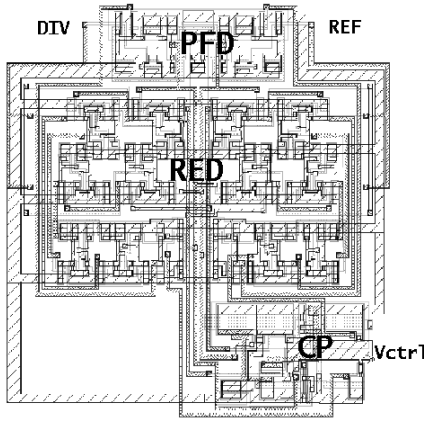

Fig. 7. The layout of the PFD, RED and Charge Pump circuits.

2) Charge Pump: The charge pump is formed by two current sources controlled by the outputs of PFD. The topology used can be seen in figure 6a. Transistors M_5 and M_6 always conduce a current proportional to the bias current I_{BIAS}, while M_1-M_4 drive the current toward the filter, X and Y nodes. This configuration is used to increase the switching speed, however, there are glitches in the output current when the UP and DN signals are activated. The transistors M_7-M_{12} force X and Y nodes at a voltage similar to V_{CTRL}, in this way the glitches due to the switching are decreased.

The second charge pump may be implemented in an easier way as shown in figure 6b, since this charge pump does not need to change its current quickly. The layout of the PFD, RED and Charge pump circuits is in fig 7.

3) Filter and Loop Variables: Loop variables are selected in order to accomplish the design specifications of the PLL, following the compromise between phase noise, lock time and stability of the loop. In this case, a typical second order passive filter has been implemented

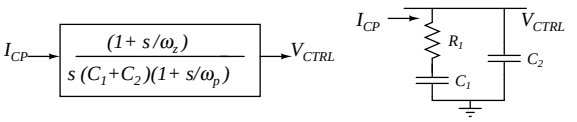

Fig. 8. Second order passive filter.

as shown in figure 8 with its transfer function. The closed loop transfer function is given by equation 1, where can be distinguished two complex poles with magnitude w_o and one real pole w_{cp}. The variables selected are summarized in table I.

$$H(s) = \frac{N(1 + s/w_z)}{(1 + s/w_{cp})(1 + s/w_oQ + (s/w_o)^2)} \quad (1)$$

TABLE I
SELECTED VARIABLES.

F_{REF}	N	I_{CP}	$K_{VCO}/2\pi$	$w_o/2\pi$	w_z/w_{cp}	Q
10MHz	1	20μA	5MHz/V	110kHz	0.9	$1/\sqrt{2}$

Based on the variables selected in table I, the filter components are calculated with the set of equations 2 and 3. The values for each component are listed in table II. The resulting phase margin was 58.36°.

$$w_{cp} = w_oQ\left(\frac{w_{cp}}{w_z} - 1\right) \quad K_n = \frac{w_o^2 w_{cp} Q}{w_o + w_{cp}Q} \quad w_p = \frac{w_{cp}w_o^2}{K_n} \quad (2)$$

$$C_2 = \frac{w_z I_{BC} K_{VCO}}{2\pi w_p N K_n} \quad C_1 = \frac{w_p C_2}{w_z} - C_2 \quad R_1 = \frac{1}{w_z C_1} \quad (3)$$

TABLE II
FILTER COMPONENTS.

R_1	C_1	C_2
5.4kΩ	3.789nF	188pF

4) VCO and Frequency Divider: For simulations, the ideal VCO provided by Eldo was used. The details of selection and design of the frequency divider are not presented because it is not the paper objective.

IV. SIMULATION RESULTS

The transient response of the PLL has been simulated with the software EldoRF of Mentor Graphics. The used transistor model was BSIM3v3, level 53, provided by Austria Micro Systems. In order to establish a comparison point, two simulations have been made, the first with the conventional PFD and the other with the proposed RED circuit.

The reference frequency was set to 10MHz, while the initial frequency of the VCO was set to 9MHz, as a result, the voltage of control goes from 1.3V to 1.5V. The average current in the case of PFD without RED is the solid line in figure 9a. In the plot can be seen when the phase error is 2π, the average charge pump

current is the maximum current. Therefore, the phase error increases and the average current starts from 0 again. This process is repeated 18 times until the phase error reach less than 2π. The transient response of the control voltage is plotted with a solid line in figure 9b. The lock time is 62μs measured with a tolerance of 1%.

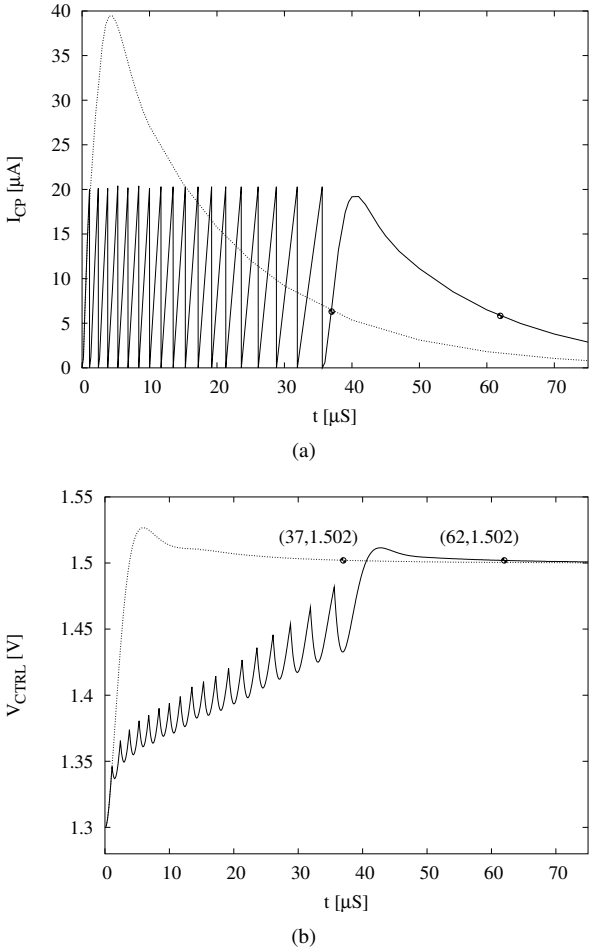

Fig. 9. Transient response of PLL with RED (dotted line) and without RED (solid line). (a) Average current. (b) Control voltage.

Under the same conditions the PLL using RED was simulated, resulting in the dashed lines of figures 9a and 9b. The waves for average current and control voltage follow the form predicted using the transfer function given by the equation 1. The lock time in this case is only 37μs.

In the steady state of the loop, the second charge pump is disabled, so it does not change the noise performance of the whole PLL. The power consumption with RED or without RED is 238μW, since the RED is not working in the locked state.

A micrograph of a full synthesizer including the proposed Phase-Frequency Detector is presented in figure 10.

V. Conclusions

A circuit that increases the detection range of the PFD of a PLL has been proposed, eliminating the cycles slip.

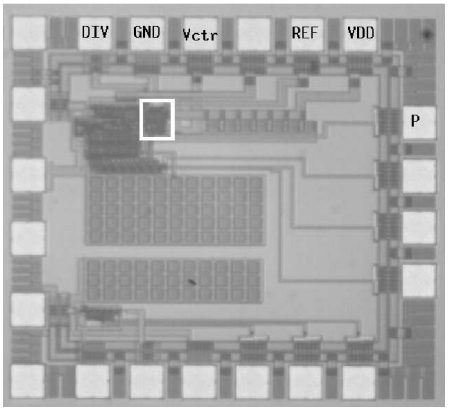

Fig. 10. Micrograph of a full synthesizer with the PFD proposed.

The circuit has low power consumption and occupies a small area. In the locked state of the PLL, the new circuit does not affect the performance of the loop. This solution is extensible to increase the detection range in a factor of 2 or more. The RED does not alter the characteristics of the loop, neither bandwidth nor gain, therefore, the stability of the loop is maintained.

References

[1] D. Banerjee and P. Boyer, "Delta Sigma *PLL*s Raise the Standard for Performance," 2003, application Brief 125, National Semiconductor.

[2] J. Lee and B. Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptative Bandwidth Control," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1137–1145, August 2000.

[3] M. I. Yiwu Tang and S. Bibyk, "A New Fast-Settling Gearshift Adaptive PLL to Extend Loop Bandwidth Enhancement in Frequency Synthesizers," *in Proc. IEEE ISCAS*, vol. 4, pp. 787–790, 2002.

[4] W.-B. Y. Kuo-Hsing Cheng and C.-M. Ying, "A Dual-Slope Phase Frequency Detector and Charge Pump Architecture to Achieve Fast Locking of Phase-Locked Loop," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 892–896, November 2003.

[5] X. Kuang and N. Wu, "A Fast-Settling PLL Frequency Synthesizer with Direct Frequency Presetting," *in Proc. IEEE Solid State Circuits Conference*, pp. 741–750, 2006.

[6] R. C. D. Dulk, "DigitaL *PLL* Lock-Detection Circuit," *Electronics Letters*, vol. 24, pp. 880–882, July 1988.

[7] W. H. Lee *et al.*, "A High Speed and Low Power Phase-Frequency Detector and Charge-Pump," *Design Automation Conf. Proc. of the ASP-DAC'99. Asia and South Pacific*, pp. 269–272, January 1999.