Introducing Asymmetry in a CMOS Latch to Obtain Inherent Power-On-Reset Behavior

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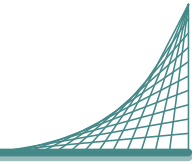
Introduction



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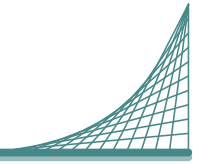

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- Initial state of sequential circuits is very important.

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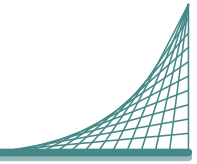

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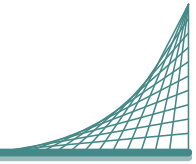

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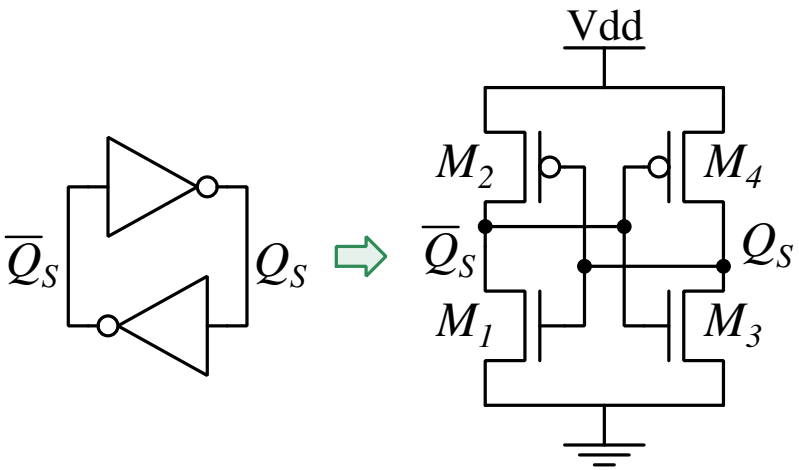
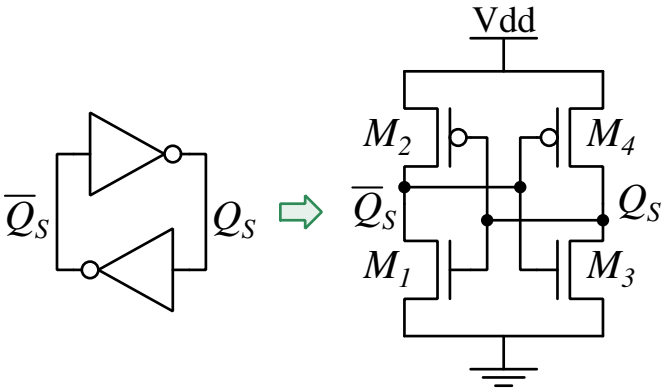
- **Reset inputs in each cell:** extra silicon area and capacitances, increasing dynamic power consumption.
- **Power-on-reset (POR) circuits:** relative large capacitors, resistors and diodes and also are designed to work under specific conditions, for example, fixed start-up time.
- We propose the use of asymmetry in a latch, turning its initial value into an well-determined state without the need of a reset.

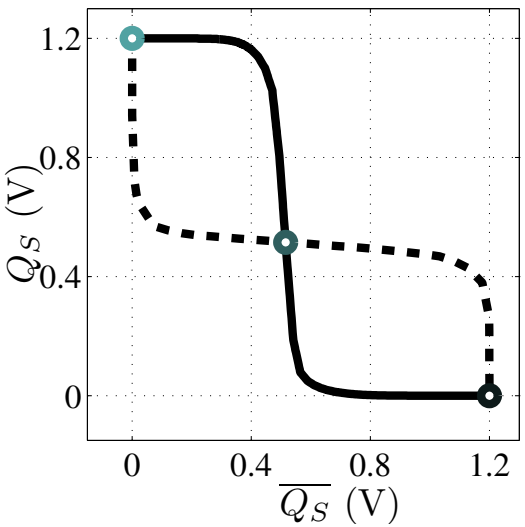
Conventional (symmetric) CMOS latch



- Mostly used in SRAM, but can be used in sequential circuits for ultra-low-power applications.

Possible states as function of the supply





Inverter transference curves: 3 intercepts

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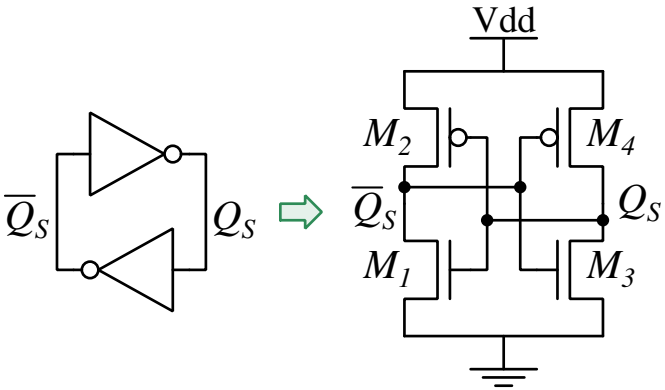

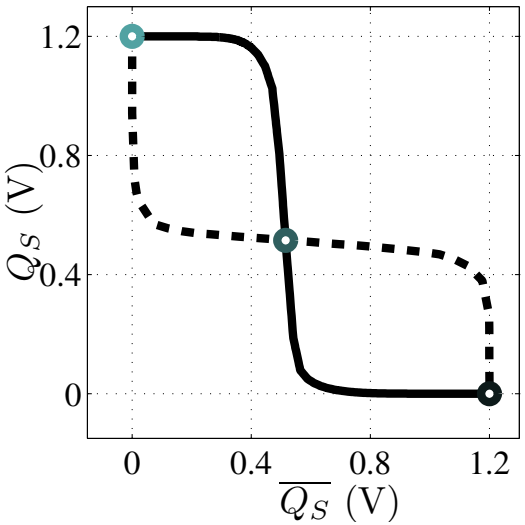

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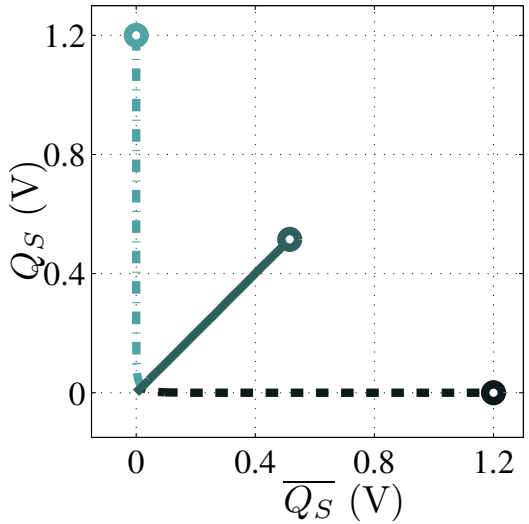

Solutions when Vdd varies from 0 to 1.2 V

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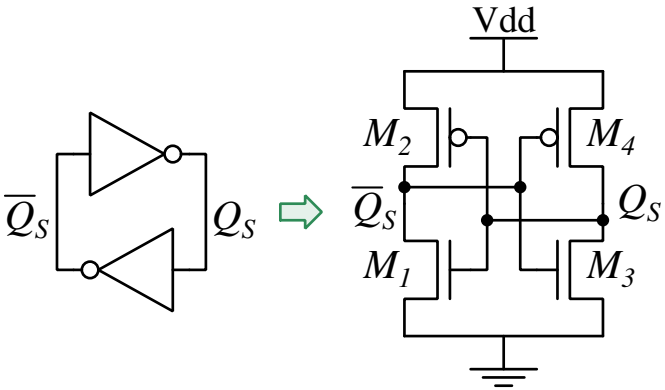

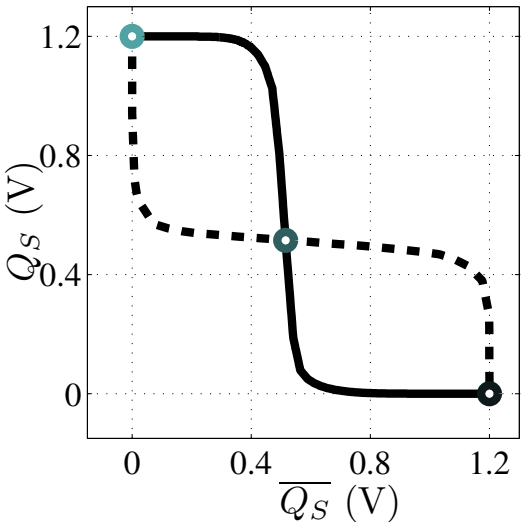

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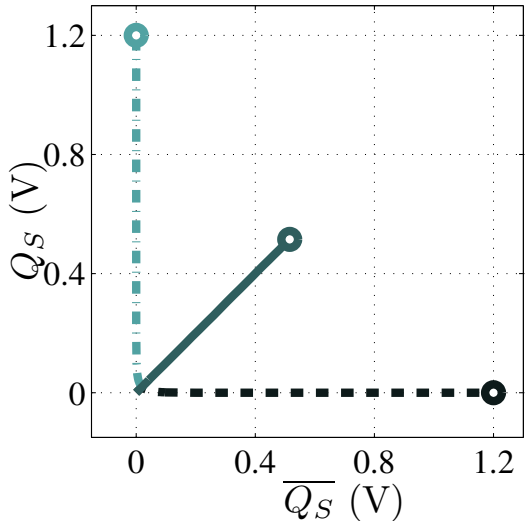

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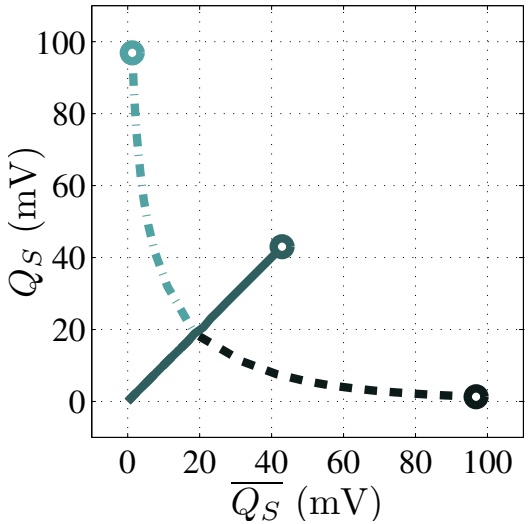
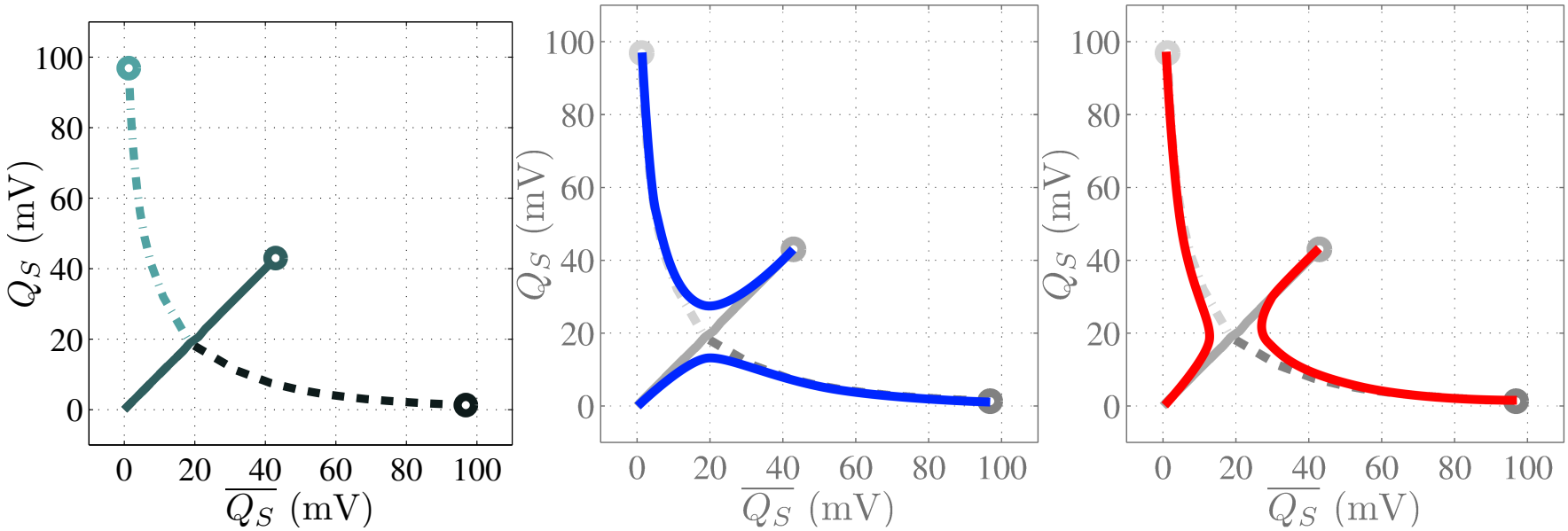


Zoom for Vdd values up to 100 mV

Decisive factors for power-on state 1

Process variations

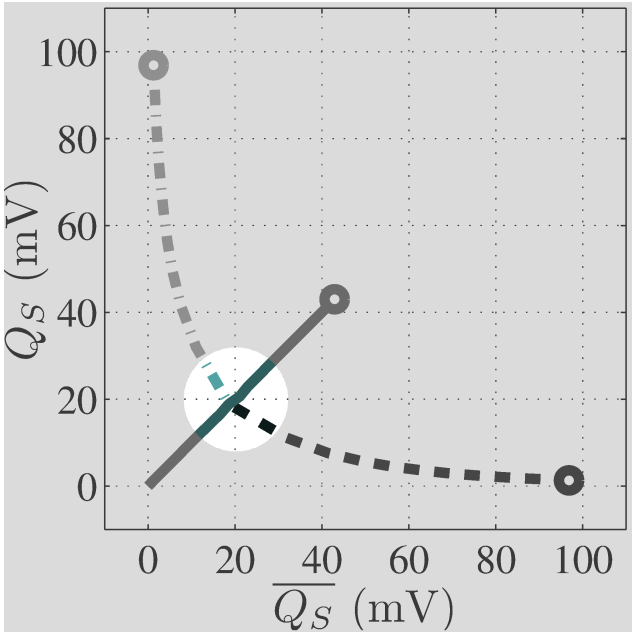


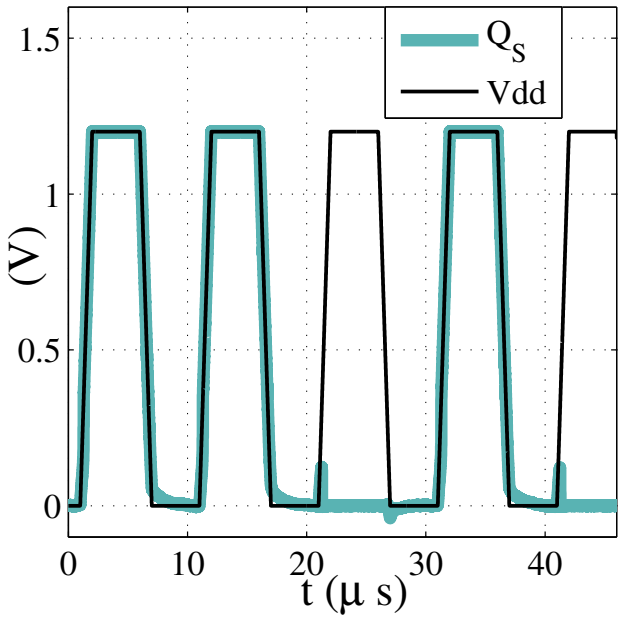
- Montecarlo simulation:

  From 300 samples, Q_S started with
  '0' in 144 samples and with
  '1' in 156 samples.

Decisive factors for power-on state 2

Noise

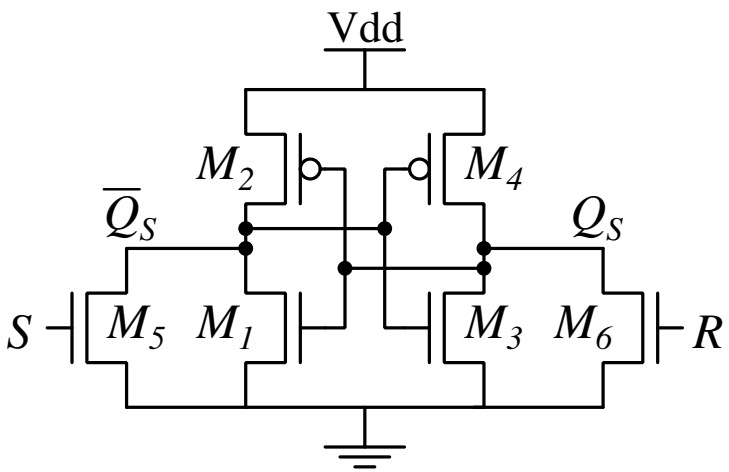




- Can be observed in a transient noise simulation.

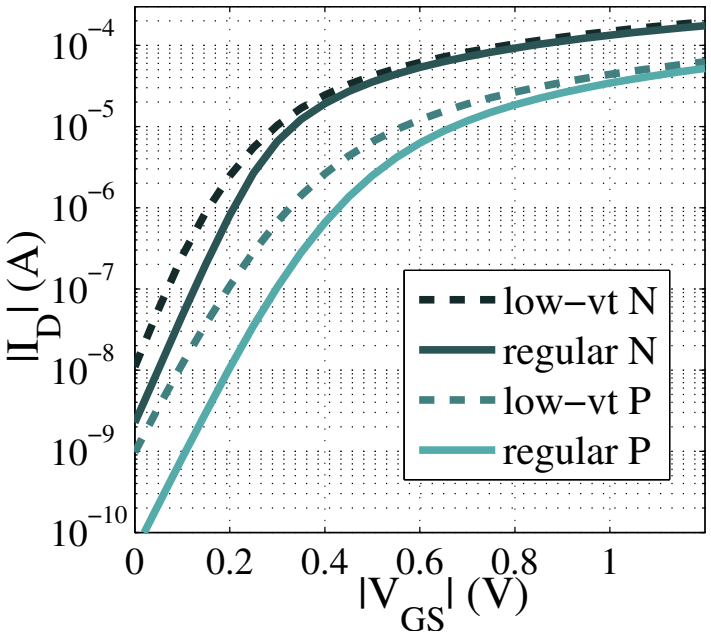
Decisive factors for power-on state 3

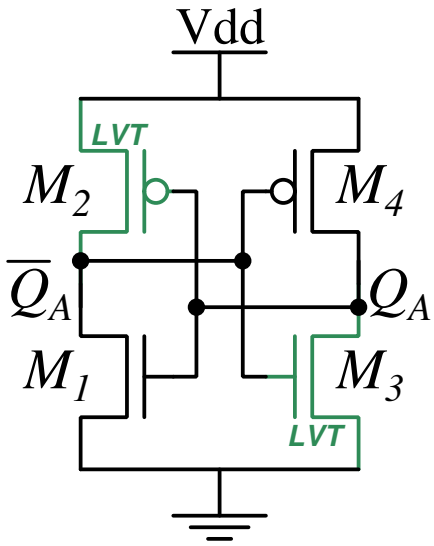
Input devices



- Unknown initial input voltages (R,S).
- Different sizes or number of transistors in each side.
- Very difficult to predict at the design stage.

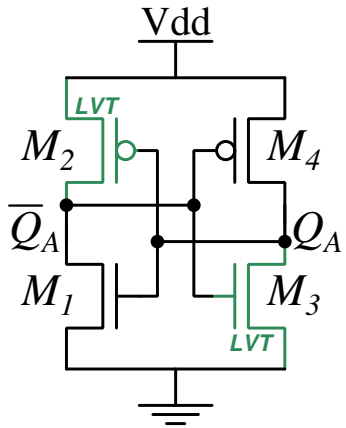
Proposed Asymmetry

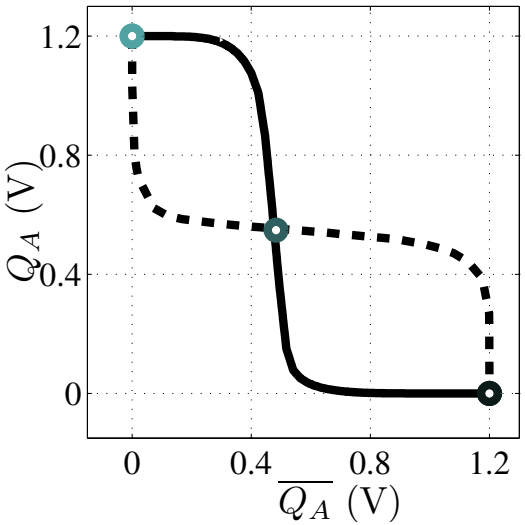




- Low-vt current $\approx$10X greater than regular transistors at $V_{GS} = 0$.

Possible states as the proposed topology





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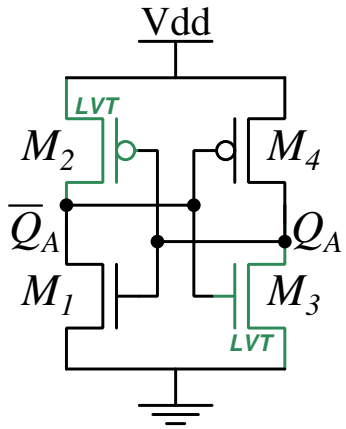

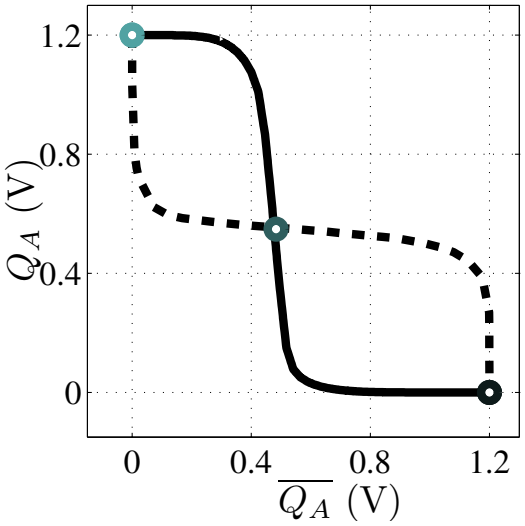

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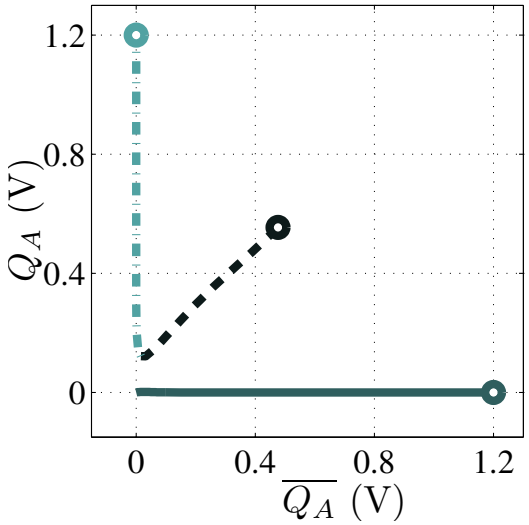

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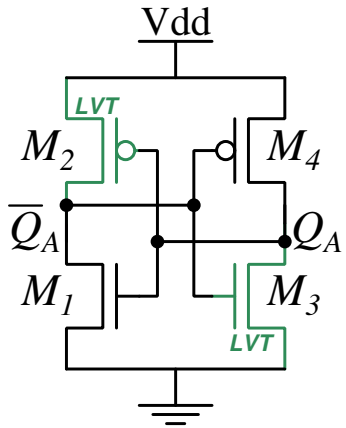

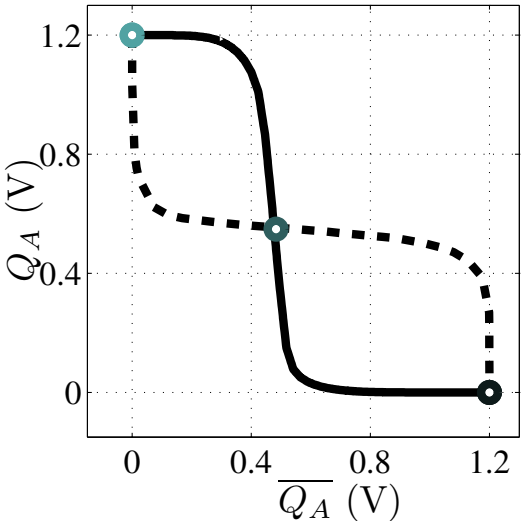

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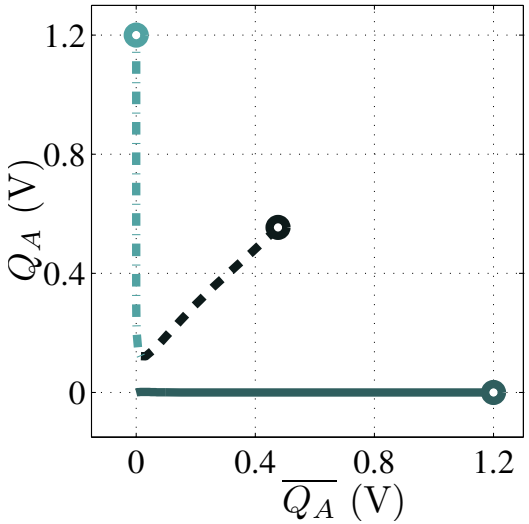

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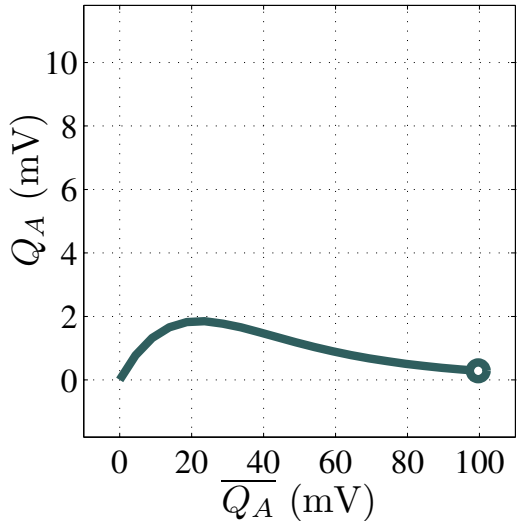
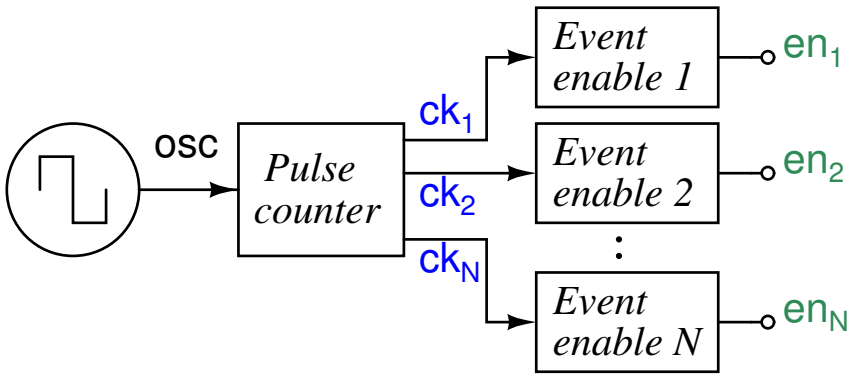
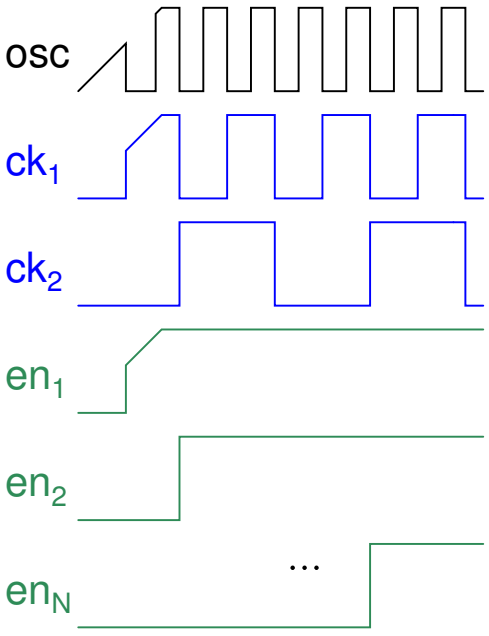
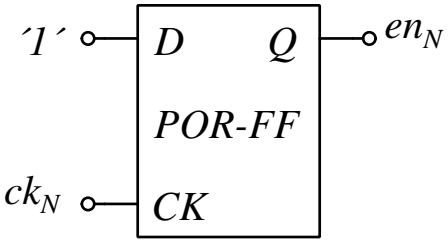


Zoom for Vdd values up to 100mV

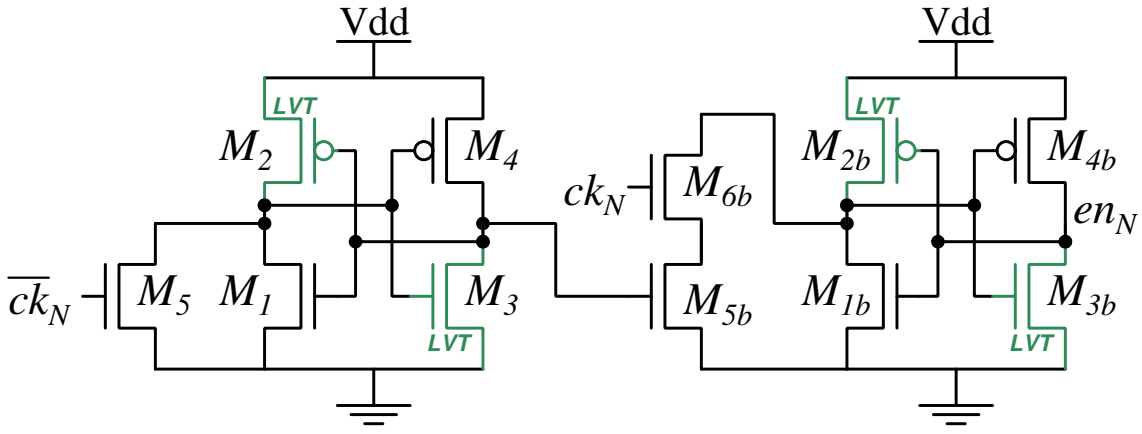
Target application used as example



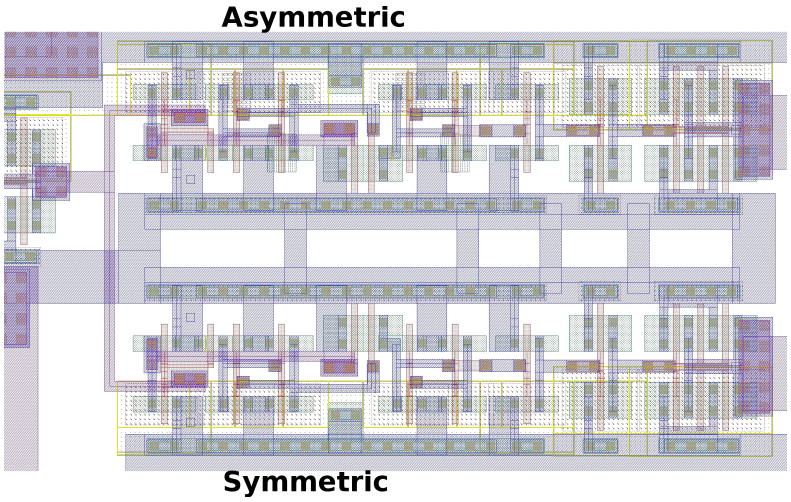


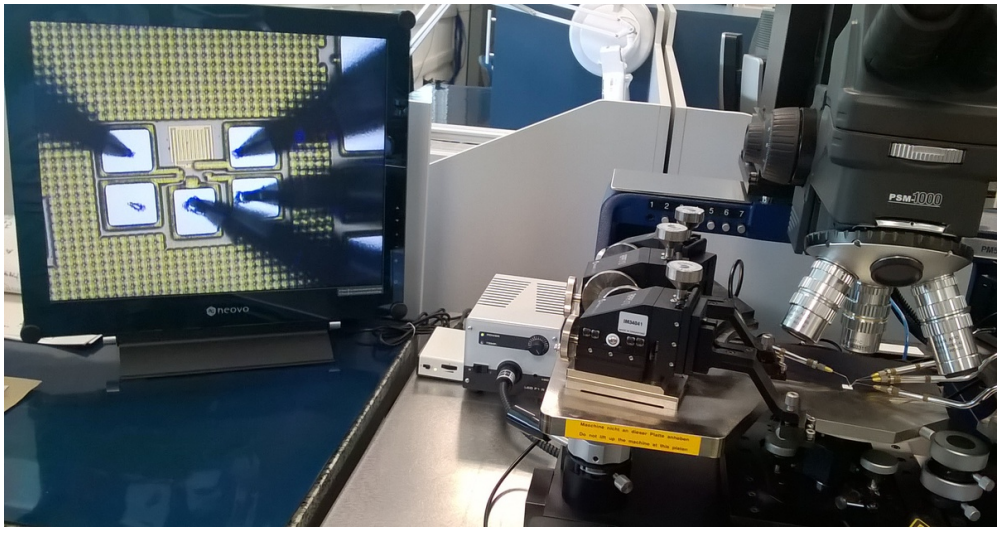


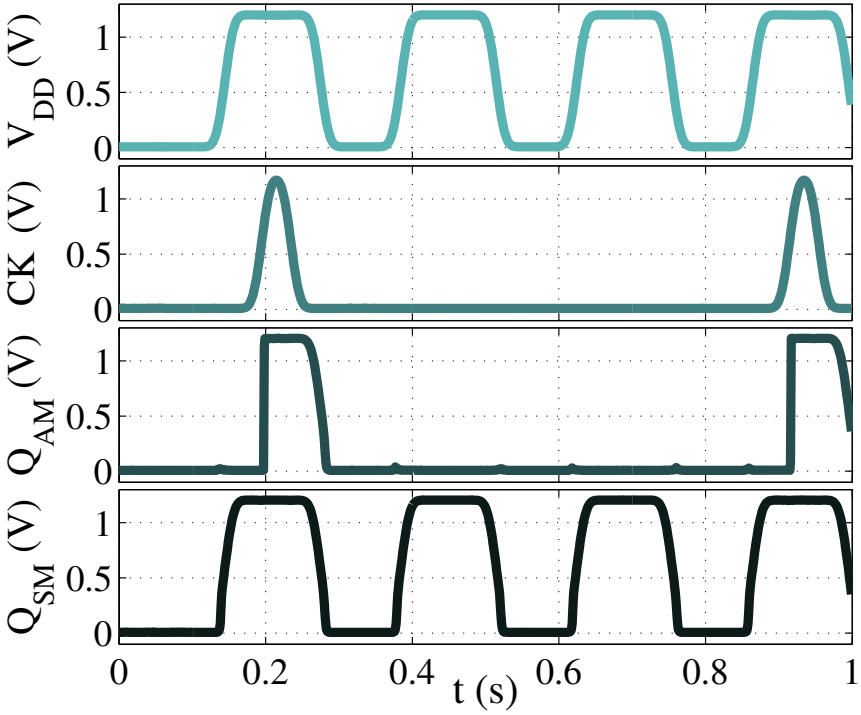
Power-On Reseted Flip-Flop



Prototype







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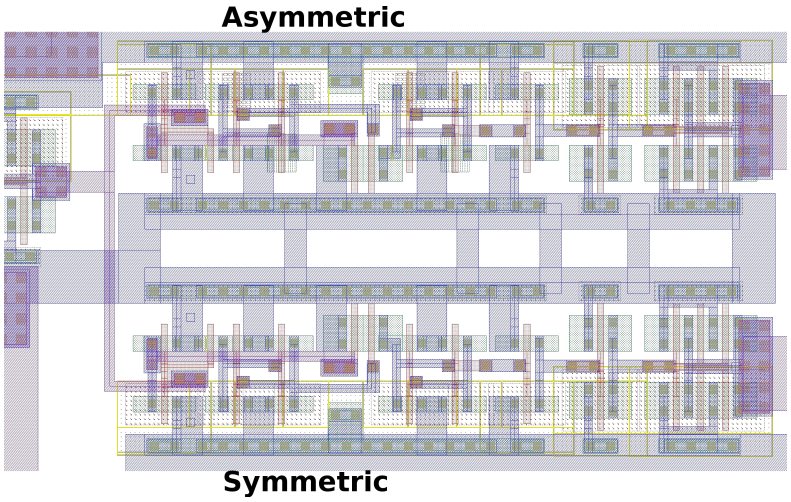
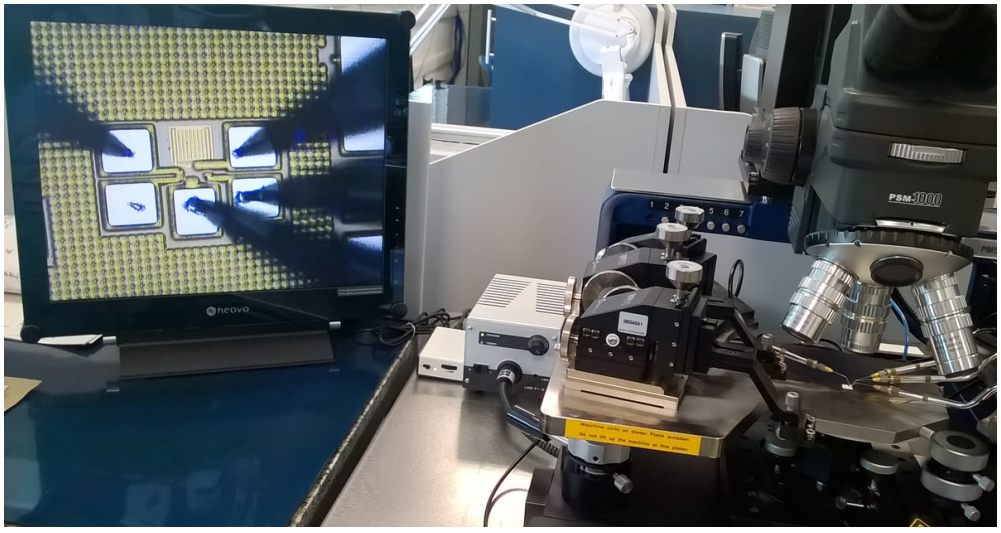
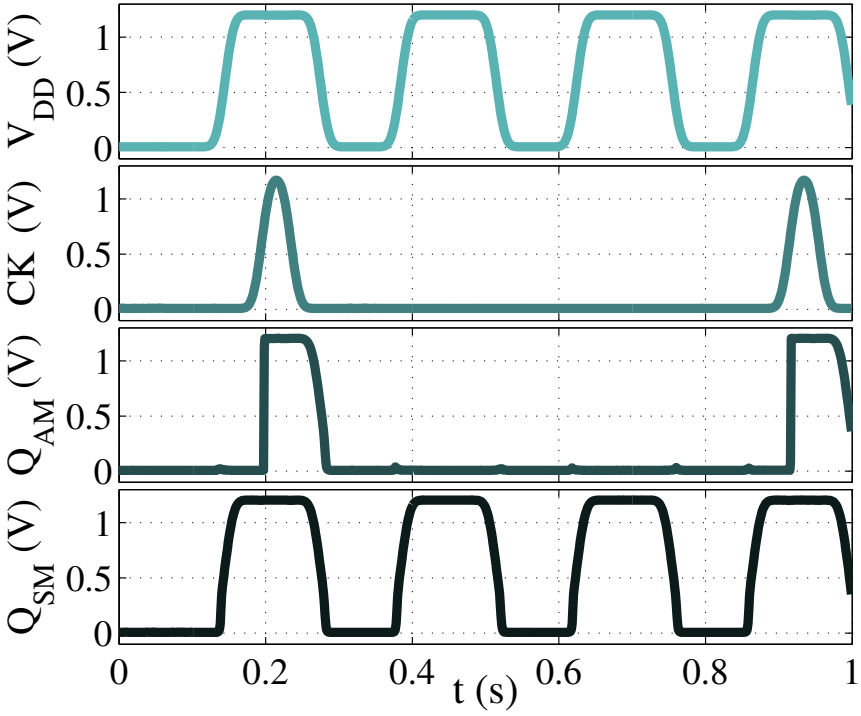




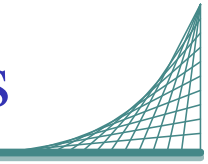


- Q_{AM} was expected to start with ‘0’. **Verified**
- Q_{SM} was unpredicted at design stage. After measurements it was concluded that **input devices** always induced an initial value of ‘1’.

Summary of the power-on characteristics of latches

	Power-on state	**Decisive factors**	**Example**
Symmetric	Variable or difficult to predict	Process variations	Montecarlo sim.
		Noise	Tran. noise sim.
		Input devices	Q_{SM} (meas.)
Asymmetric	Imposed by design	Design	Q_{AM} (meas.)

Conclusions



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- We can impose by design the initial value of a latch using asymmetry. This can be done with different threshold-voltage transistors.
- The proposed modification kept the same occupied area and had little effect on propagation times.
- A new block called **Power-on Reseted Flip-Flop (POR-FF)** was designed and tested in CMOS 130nm, verifying its correct functioning.
- This technique has the advantage of avoiding power-on reset module and reset inputs in each sequential cell. (lower occupied area and lower dynamic power consumption)

Questions?